K+K FDI

Digital Input supplement to FXE phase meter

Manual

Issue: Aug. 2012, Version 13-22-25

Revision History

120813	initial version
130225	corrected supply voltage on DIN 41612 connectors to 716V (p.4. §2) added AC-coupling of load resistor (p.4, §4)
	corrected 'Output with Bits 1631' to 1kHz (preliminary specifications)

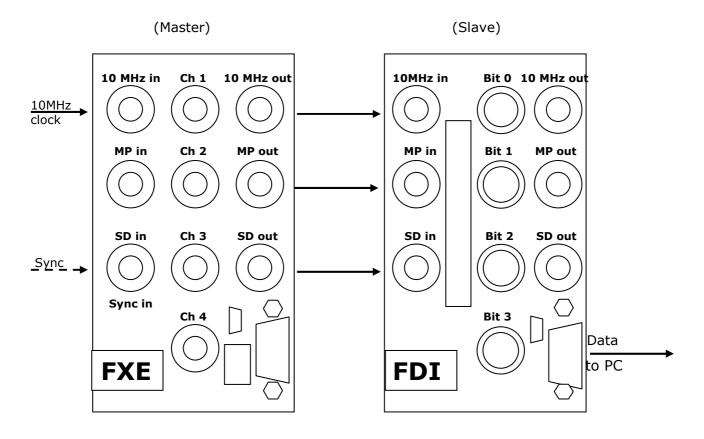
Description of the Digital Input board "FDI"

The FDI board provides 32 digital inputs to be sampled synchonously with the phase measurements from the FXE boards, to which it is a supplement.

The board has the same mechanical format as the FXE boards, the same pinout with respect to power supply, Scrambler and Sync connections, and the same front panel SMA connectors for chaining with other FXE and/or FDI boards. Therefore, FXE and FDI boards may be inserted into the same slots.

FDI boards can only be used as a slave, following one or more FXE boards. Therefore, they do not have a Master/Slave jumper, they can not be equipped with a Scrambler and they do not have a sync input. However, they will respond to a sync from the master board just as slave FXE boards do.

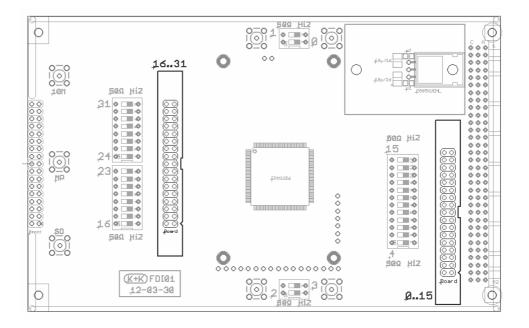
One FDI board contributes as many bytes to the data stream as a single FXE channel. Therefore, the limit of 24 FXE channels is reduced to 20 FXE channels, if 1 to 4 FDI boards are part of the chain of boards. Current firmware cannot recognize more than 4 FDI boards in a chain.



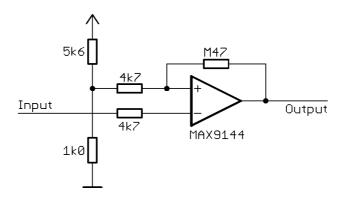
Description FXE Phase Meter Version: 13-02-25 Last Update: 12-08-13 Page 3/7 K+K Messtechnik GmbH, St-Wendel-Str. 12, D-38116 Braunschweig, Tel: +49(0)531/501436, kplusk@t-online.de

Short description of the Digital Inputs/Outputs:

- 1. There are two on-board 34-pin DIN 41612 connectors for <u>Bits 0..15</u> and for <u>Bits 16..31</u>. Besides the respective bit inputs, each connector provides a single output which as a default delivers the 10MHz reference clock with Bits 0..15 and the once-per-millisecond raw measurement trigger with Bits 16..31. These output signal may easily be modified by changing the FPGA configuration.
- 2. To reduce cross talk and to supply optional custom specific input conditioning hardware, adjacent signal pins are separated by either GND pins or regulated 5V or unregulated 7..16V supply pins -- see below for the pinout.



- 3. For versatility, Bits 0..3 are also accessible via BNC connectors at the front panel. Bits 4..15 and the corresponding output are also connected to the back panel connector. A copy of the Bits 16..31 DIN 41612 connector is available at the front panel.
- 4. For each input bit there is a DIP switch to (dis)connect it to/from a 50 Ohm load resistor which is AC-coupled to GND by a 100nF capacitor. The switches are located close to the DIN connectors and labelled with the respective bit numbers. For Bits 0..3 they are located close to the respective coax connectors.
- 5. Comparator Input Circuit:



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Pinout of the 96-pin backplane connector:

Power Supply:

1 a+b+c: unused, may be connected to +14...16V for compatibility with FXE

5 a+b+c: +5V (regulated) out

7 a+b+c: +7V...16V (unregulated) in

Signals needed only for **concatenation of several boards** via backplane connector:

9a: Reset SCR (it is recommended

9c: Clock SCR to add a GND connection)

10c: Up/Down SCR

30a: Sync (it is recommended

30c: Enable to add a GND connection)

RS232 port:

26a: RXD RxD from PC 26c: TXD TxD to PC

USB: not available on backplane connector

2, 4, 6, 8, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 32 (each a+b+c): GND

Input/Output bits:

12c: Output with Bits 0..15 (Default: 10MHz)

14c: Input Bit 15

14a: Input Bit 14

16c: Input Bit 13

16a: Input Bit 12

18c: Input Bit 11

18a: Input Bit 10

20c: Input Bit 9

20a: Input Bit 8

22c: Input Bit 7

22a: Input Bit 6

24c: Input Bit 5

24a: Input Bit 4

Bits 0..3 are connected to front panel BNC connectors

All other pins are either unconnected or reserved - leave them unconnected!

Pinout of the Bits 0..15 DIN 41612 connector:

```
2:
        Input Bit 0
4:
        Input Bit 1
                            Bits 0..3 are also connected to front panel BNC connectors
6:
        Input Bit 2
8:
        Input Bit 3
10:
        Input Bit 4
12:
        Input Bit 5
14:
        Input Bit 6
16:
        Input Bit 7
18:
        Input Bit 8
20:
        Input Bit 9
                             Bits 4..15 are also connected to the backplane connector
22:
        Input Bit 10
24:
        Input Bit 11
26:
        Input Bit 12
28:
        Input Bit 13
30:
        Input Bit 14
32:
        Input Bit 15
34:
        Ouput with Bits 0..15 (Default: 10MHz)
1, 5, 9, 13, 17, 21, 25, 29, 33: GND
3, 7, 11, 15, 19:
                     regulated 5V
23, 27, 31:
                  unregulated 7..16V
```

Pinout of the Bits 16..31 DIN 41612 connector (both on-board and Front Panel):

```
2:
        Input Bit 16
4:
        Input Bit 17
6:
        Input Bit 18
8:
        Input Bit 19
10:
        Input Bit 20
12:
        Input Bit 21
14:
        Input Bit 22
16:
        Input Bit 23
18:
        Input Bit 24
20:
        Input Bit 25
22:
        Input Bit 26
24:
        Input Bit 27
26:
        Input Bit 28
28:
        Input Bit 29
30:
        Input Bit 30
32:
        Input Bit 31
34:
        Ouput with Bits 16..31 (Default: Measurement pulse)
1, 5, 9, 13, 17, 21, 25, 29, 33: GND
3, 7, 11, 15, 19:
                     regulated 5V
23, 27, 31:
                   unregulated 7..16V
```

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Preliminary specifications:

Input 'high' level: 1,0 .. 5,0 V
 Input 'low' level: 0,0 .. 0,5 V

- A short positive input pulse (>50ns) will set the respective bit to '1' for the current millisecond's raw measurement
- A single raw measurement within the report interval with a bit '1' will cause a '1' to be reported.

• Output with Bits 0..15: 10MHz reference clock, 5V, 1:1 duty cycle

• Output with Bits 16..31: Measurement pulse (1kHz, 5V, 71:29 duty cycle)

• Temperature range: 0...+50 °C

• Supply voltage: +5V reg. (or 8V unreg.), +12V reg. (or 15V unreg.)

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